Thick and Thin Film Materials Based Chip Level Packaging for High Temperature SiC Sensors and Devices

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Abstract

Gold thick-film material was used for electrical interconnections (thick film printed wires and thick film metallization based wire-bond) and conductive die-attach for high temperature (up to 500 ^{o}C) chip level packaging. During a 1500-hour test in atmospheric oxygen with and without bias, these basic interconnection elements demonstrated low and relatively stable resistance at both room temperature and 500 ^{o}C. A SiC test diode with an annealed nickel thin-film ohmic contact on the backside was successfully attached to a ceramic substrate using gold thick-film material as conductive bonding layer. The attached SiC diode has been tested at 500 ^{o}C in oxidizing air for 1000 hours. The upper limit of electrical resistance of the die-attach interface estimated by forward dynamic resistance of the attached diode, during and after the high temperature test, remained desirably low and stable over the entire course of a 1000-hour test.

I. Introduction

Single crystal silicon carbide (SiC) possesses such excellent physical and electronic properties (wide energy gap and low intrinsic carrier concentration) that SiC based semiconductor electronics can operate at temperatures in excess of 600 ^{o}C, well beyond the high temperature limit for Si based semiconductor devices. Various SiC semiconductor devices have recently been demonstrated to be operable at temperatures as high as 600 ^{o}C,[1, 2] but only in a probe-station test environment partially because chip level packaging technology for high temperature devices (500 ^{o}C and beyond) is not available (still in development). Core technologies needed for successful high temperature electronic packaging are high temperature operable electrical interconnections and die-attach. For decades, precious metal thick-film metallization (on ceramic substrates) have been used for hybrid-packaging traditional (room temperature to 150 ^{o}C) electronics. Recently, gold (Au) based thick film materials, which are normally processed at high temperatures (850 ^{o}C), have been tested for electronic packaging techniques to achieve 500 ^{o}C operation.[3, 4, 5] This paper reports test results, at both room and elevated temperatures, of thick- and thin-film based electrical interconnection components and low resistance die-attach scheme operable up to 500 ^{o}C in oxidizing air environment.

II. Thick Film Material

Thick film metallization materials are usually composed of (1) fine metal (such as gold) powder, (2) inorganic binder (such as metal oxides), and (3) organic vehicle. Screen printing technique is usually used for thick-film coating with thickness control. During the initial drying process (at ~150 ^{o}C) the organic vehicle evaporates and the paste becomes a semi-solid phase mixture of metal powder and binder. In the following curing process (~ 850 ^{o}C recommended by DuPont for best adhesion on an alumina substrate) the

inorganic binder molecules migrate to the metal/substrate (e.g. Au/ceramic) interface and form reactive binding chains. Au thin wires can be bonded directly to Au thick film metallization pads to provide electrical interconnection in packaging. Some new thick film materials (DuPont5771) may be applicable to various ceramic substrates such as alumina (Al_2O_3) and aluminum nitride (AlN).[6] Because of the wide application in hybrid-packaging (at T < 150 ^oC) the electrical and mechanical properties of commercial thick film materials have been well validated for room temperature application. In this work thick-film material based electrical interconnections (thick film printed wires and thick film metallization based wire-bond) and conductive die-attach scheme were systematically evaluated for operation up to 500 ^oC.

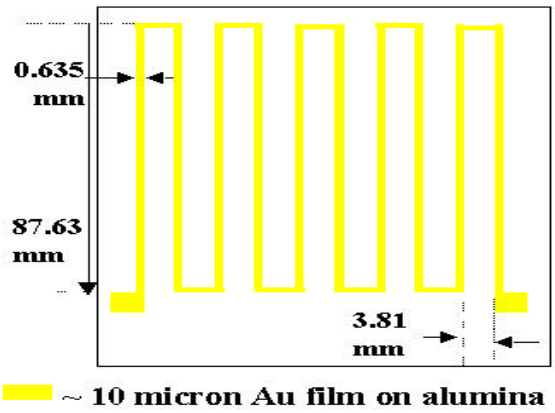

Figure 1: Schematic diagram of screen-printed thick film wire for resistance and stability tests at various temperatures.

III. Electrical Interconnections

1. Thick Film Printed Wire

Au based thick film was used as metallization of ceramic substrates, such as AlN and 96% Al_2O_3. Commercialized thick film materials have been widely used in hybrid-packaging so both electrical and mechanical properties at room temperature have been thoroughly validated. In this work, Au thick film (DuPont5771) printed wire was first tested at 500 ^oC in oxidizing air with and without electrical current flow. The thick film printed wire, as shown in Figure 1, was screen printed on a ceramic substrate (96% Al_2O_3) and cured at 850 ^oC in air using the recommended curing process.[6] The circuit was tested at 500 ^oC in air for a total of ~1500 hours. The electrical resistance of the thick film wire/circuit was first measured at room temperature. After that, the temperature ramped up to 500 ^oC for ~1000 hours without current flow and the resistance of the wire was measured periodically. The resistance slightly fluctuated within 0.1% during the 1000 hours. After testing for 1000 hours without current, the circuit was biased with 50 mA DC current and the resistance was continuously monitored. The resistance kept fluctuating slightly within 0.1% for 500 hours with bias. This very small change in resistance is acceptable for almost all envisioned high temperature electronic application.

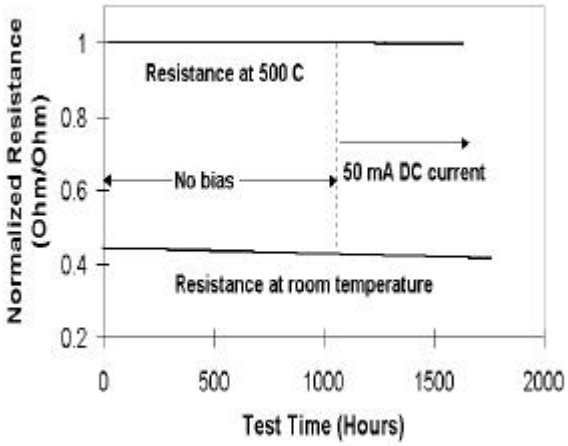

Figure 2: Normalized resistance of thick film wire at various temperatures with and without DC bias.

2. Thick Film Based Wire-bond

The electrical test circuit including thick-film (DuPont 5771) printed wires/pads and thin gold wires bonded to the pads is illustrated in Figure 3. The geometry of the conductive wires and the metallization pads were so designed that the electrical resistance of test circuit is dominated by the resistances of thin (0.0254 mm diameter) bonded gold wires. The thick film conductive wires/pads were processed according to standard drying and curing processes (Processing and Performance Data of DuPont Thick Film Materials) suggested by the material manufacturer. The thin gold wires were bonded to the thick-film pads on substrate by thermal-press wire bonding technique.

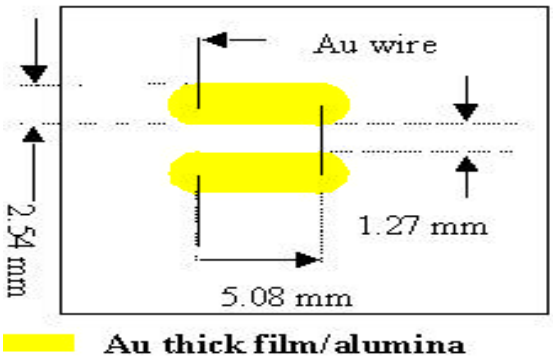

Figure 3 Schematic diagram of one unite of thick film metallization based wire-bond test circuit. 0.0254 mm (0.001") Au wires were bonded to thick film pads using thermal press technique.

The electrical resistance of thick-film metallization based wire-bond test structure (illustrated in Figure 3) include those of thick film conductive wire/pads and bonded thin Au wires and the interfaces between them. The resistances of 22 units (44 bonds) in series were measured at room temperature and 500 ^{o}C versus accumulated testing time. The resistance was first measured at room temperature, following which the temperature was ramped to 500 ^{o}C and the resistance was monitored in air without bias for 670 hours. The temperature was then reduced back to room temperature and the resistance was recorded again. After this thermal cycle, the circuit resistance was continuously monitored for a total of 1200 hours at 500 ^{o}C in air without current flow, followed by another 500 hours at 500 ^{o}C with 50 mA (DC) current. The resistances under all these conditions were desirably low (less than 0.5 Ω) and slightly decreased at an average rate of 2.7% over 1500 hour testing period. The rate of resistance decrease under the DC bias is close to that without bias.

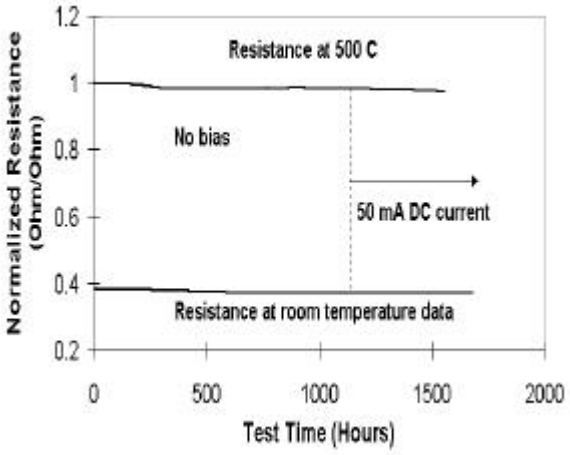

Figure 4: Normalized resistances of wire-bond test circuit measured at room temperature and 500^{o}C vs. test time at 500 ^{o}C with and without DC bias.

IV. Conductive Die-attach

1. SiC Device Fabrication

N-type (nitrogen, resistivity less than 0.03 Ω-cm) Si terminated 4H-SiC wafer was used for test device fabrication. The backside wafer (unpolished side) was first coated with a nickel (Ni) thin film (~ 6000 Å) by electron beam evaporation. The SiC wafer was then

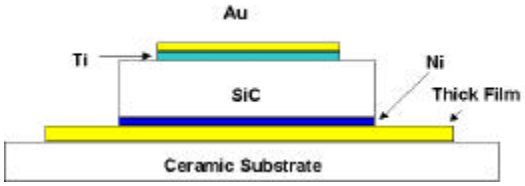

Figure 5: Schematic diagram of as-fabricated SiC device and die-attach structure.

annealed at 950 ^{o}C in argon in a tube furnace for 5 minutes forming an ohmic contact on the backside of the SiC wafer. Following the annealing, a second layer (3000 Å) of Ni was electron beam evaporated onto the wafer backside. The device structure on the front side of the SiC wafer was fabricated by electron-beam evaporation of thin (100 Å) titanium (Ti) and Au thin (4000 Å) films on cleaned SiC wafer and patterned with the liftoff technique. The Ti interlayer was used to improve interfacial adhesion of metal thin film on the polished front side of SiC.

2. Conductive Die-attach

After dicing, the 1 mm x 1 mm diode chips were then attached to a ceramic substrate (either AlN or alumina) using DuPont 5771 Au thick-film material. This thin and thick film process for SiC device results in a low resistance die-attach structure which is needed for packaging many devices, especially, Schottky diode based sensors/circuits and power devices with vertical topologies.

A SiC test die with a Ni contact on the back was attached to a ceramic substrate using an optimized two-step Au thick-film processing.[5] A thick film layer was first screen-printed on the substrate and cured at 850 ^{o}C. The SiC die was then attached to the cured thick film pattern with minimal amount of subsequent thick film. A slower drying process (120 ^{o}C – 150 ^{o}C) was critical to keep the thick-film bonding layer uniform and the die parallel to the substrate after the curing process. Following the drying, the attached die was processed at a lower final curing temperature (600 ^{o}C).

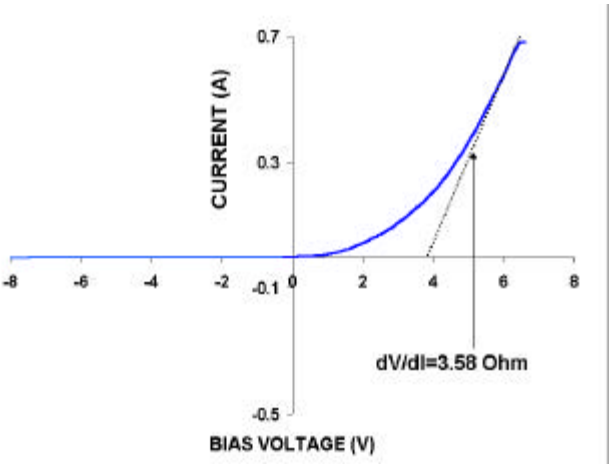

Figure 6: I-V curve of attached SiC test-diode characterized at 500 ^{o}C after being tested for 1000 hours at 500 ^{o}C oxidizing air.

As was discussed previously, this optimized Au thick film die-attach process allows sufficient diffusion of inorganic binders towards the thick film/substrate interface resulting in a good strength of binding to the ceramic substrate. Meanwhile, it allows the attached semiconductor chip not to be exposed to temperatures higher than the ultimate operation temperature of SiC devices (600 ^{o}C) during the die-attach process. The second advantage of this die-attach process is that the distribution of the thick film (after the final curing) between the chip and the substrate can be better controlled because only a minimal amount of thick film material is necessary to attach the chip to a cured thick film pad. Therefore, many possible problems caused by non-uniform thick film distribution at chip/substrate interface can be avoided.

An Au 0.001" diameter wire was bonded on the top Au thin-film metallization pad with a thick-film overlayer by thermal-press bonding technique. Thick film material was also used to reinforce the top Au thin film for better wire bonding. The Au thin-film metallization area was coated with thick film on the top then dried at 150 ^{o}C for 10 minutes. The thick film on the device top was cured during the final die-attach process (at 600 ^{o}C).

The attached SiC test diode (Figure 5) was characterized by current - voltage (I-V) measurements at both room temperature and 500 ^{o}C and for various heating times. A minimum dynamic resistance (dV/dI) in a high current (forward biased) region of the I-V curve was used to estimate both the stability and the upper limit of resistance of the die-attach structure (both interfaces and materials), as shown in Figure 6. This dynamic resistance includes forward dynamic resistance of Au/Ti/SiC interface, SiC wafer bulk resistance, the die-attach materials/ interfaces resistance, bonded wire resistance, and the test leads resistance in series. The resistance contributed from test leads and bonded wire were measured independently and subtracted. The attached device was first characterized with I-V measurements at room temperature. The device exhibited rectifying behavior and the lowest dynamic resistance after subtracting test-leads/bond-wire resistance (applies to all the following discussion) measured under forward bias was ~ 2.6 Ω, as shown in Figure 7. The temperature was then ramped up to 500 ^{o}C (in air) and the diode was *in situ* characterized periodically by I-V measurement for ~1000 hours. During the first 70 hours at 500 ^{o}C the (lowest) dynamic resistance under forward bias increased slightly from 3.3 Ω to 3.8 Ω. After that the dynamic resistance decreased slightly and remained at an average of 3.1 Ω. The diode was then cooled down to room temperature and characterized again. The lowest forward dynamic resistance measured at room temperature was 3.3 Ω. It is worth noting that the device's I-V curve changed somewhat with time during heat treatment at 500 ^{o}C. However, the dynamic resistance of attached diode remained comparatively low over the entire duration of the test and temperature range, indicating a low and relatively stable die-attach resistance.

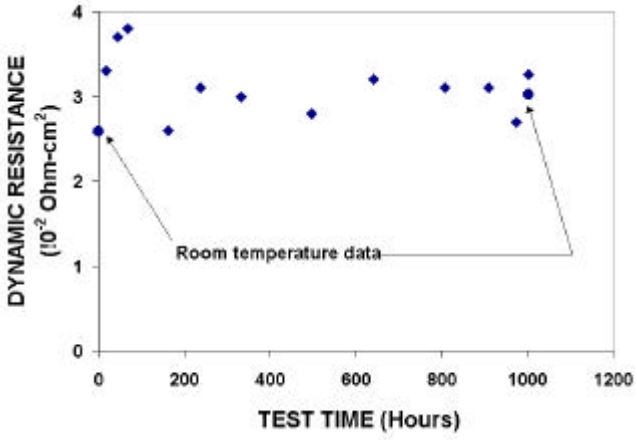

Figure 7: Minimum specific dynamic resistance (normalized to device area) calculated from I-V data vs. heating time at 500 ^{o}C. This resistance includes resistances contributed from the Au(Ti)/ SiC rectifying interface, SiC wafer, the die-attach materials/interfaces. Resistances of the bonded wire and the test leads have been subtracted.

V. Summary and Discussion

Au thick film (DuPont 5771) based electrical interconnections (thick film printed wires and thick-film based wire bond) were electrically tested at 500 ^{o}C with and without bias in oxidizing environment for 1000 hours for application in high temperature chip level packaging. The resistances of these basic electrical interconnections were low and relatively stable. A SiC test chip (diode) with backside Ni thin-film metallization was

successfully attached to ceramic substrates using Au thick film as a conductive bonding layer. During the entire test time period of 1000 hours at 500 ^{o}C the attached SiC test diode demonstrated excellent rectifying behavior in the oxidizing air environment. The stable (lowest) forward resistance of the attached diode at 500 ^{o}C during the entire testing period indicated satisfactory performance of die-attach at 500 ^{o}C.

The chemical behavior of Au/Ni/SiC system at 500 - 600 ^{o}C, especially, in oxidizing environment, has not been investigated. It will be critically important to understand both metallurgical and chemical behaviors of this system in order to predict the electrical properties of this SiC die-attach structure for longer term (~ 10^4 - 10^5 hours) operation.

Recently, a thin film ohmic contact system with a diffusion barrier layer for SiC high temperature devices was reported.[7] It is worthwhile to compare this multi-layer thin-film contact system with Ni ohmic contact for die-attach application.

The room temperature mechanical properties of thick film metallization on various substrates, Au wire-bond on Au thick-film, and SiC semiconductor die-attach using thick-film materials have been evaluated previously.[1, 4] However, equivalent mechanical tests at elevated temperatures remain to be carried out in future planed work in order to more completely validate thick film material application for high temperature electronic packaging.

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